REMARKS

The Examiner is thanked for the thorough examination of the present application, the allowance of claim 10-15 and the indication that claim 18 contained allowable subject matter. Applicants have amended claim 18 to incorporate the contents of claim 16, and thereby place claim 18 in independent form and in immediate condition for allowance. In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all claims are in condition for allowance.

Specifically, in this Amendment, Applicants have amended claims 16 and 18. Claims 1-9 are cancelled in accordance with the previous election. And, claims 21-26 are added for further protection. The title of the invention is amended herein to be clearly indicative of the invention to which the claims are directed (as method claims have been canceled). After entry of the foregoing amendments, claims 10, 16 and 18 are independent claims, and claims 10-26 are now pending in the application.

As claim 18 (admitted to contain allowable subject matter) has been amended to place it in independent form such, claim 18 and claims 23-26 depending therefrom are now in condition for allowance.

Claims 16-17 and 19-20 were tentatively rejected under 35 U.S.C. 102(e) as allegedly anticipated by Lai (U.S. Patent No. 6,825,497). Claim 16 has been amended, and the amendment to claim 16 renders the rejection moot. Specifically, claim 16 has been amended to claim "wherein at least one of the source electrode and the drain electrode is positioned on a part of the second insulation layer." This feature clearly defines claim 16 over the cited art of record.

It is well settled that a reference may anticipate a claim within the purview of 35 USC section 102 only if all the features and all the relationships recited in the claim are taught by the reference structure either by clear disclosure or under the principle of inherency.

Applicants' independent claim 16 recites a thin film transistor substrate, including a plurality of stack structures on the substrate, an ohmic contact layer, a second insulation layer, a source electrode and a drain electrode, a passivation layer, and a transparent conduction layer. Each stack structure includes layers successively disposed, which are a first conduction layer, a first insulation layer, and a semiconductor layer. The ohmic contact layer is positioned on a first region and a second region of the semiconductor layer, where the first region and the second region are disconnected. The second insulation layer is positioned at least on side surfaces of the stack structures. The source electrode is positioned at least on the ohmic contact layer in the first region, and the drain electrode is positioned at least on the ohmic contact layer in the second region. **At least one of the source electrode and the drain electrode** is positioned **on** a part of the second insulation layer. The passivation layer is positioned on the semiconductor layer and the source and the drain electrodes. The transparent conduction layer is positioned on the passivation layer and electrically coupled to one of the source and the drain electrodes.

In contrast, *Lai et al.* disclose an active matrix substrate for a liquid crystal display including gate lines 13, a patterned gate insulating layer 15a, a patterned semiconductor layer 17, a patterned n-doped layer 19, a low k dielectric layer 23, source electrodes 21S and drain electrodes 21D, and a passivation layer 27. The low K dielectric layer 23 is formed on the source electrodes 21S and drain electrodes 21D and the transparent substrate 11. The passivation layer 27 is formed on the conducting lines 25b, and the channels between the source electrodes 21S and the drain electrodes 21D. (FIG. 7E; Col. 4, lines 42-46; and Col. 5, lines 7-11)

However, there is no disclosure (or even a suggestion) by *Lai et al.* that at least one of the source electrode and the drain electrode is **positioned on** a part of the second insulation layer, as recited in claim 16. Instead, the low K dielectric layer 23 of *Lai et al.*, relied upon by the Examiner as being the second insulation layer, is formed on the source electrodes 21S and drain electrodes 21D. (FIG. 7E; Col. 4, lines 45-46) As is clear from FIG. 7E, the spatial relationship of the source/ drain electrodes 21S/ 21D and the alleged second insulation layer 23 is opposite (e.g., upside-down) from that of the invention defined in claim 16. That is, the source electrodes 21S and drain electrodes 21D of *Lai et al.* is disposed under the low K dielectric layer 23 conversely.

As such, the structure of claim 16 is not disclosed (nor is it suggested) by *Lai et al.* Therefore, claim 16 is not anticipated (or rendered obvious) by the cited reference. Moreover, since claims 17 and 19-20 depend from claim 16, claims 17 and 19-20 also are not anticipated (or rendered obvious) by *Lai et al.* Accordingly, the rejection of these claims should be withdrawn.

For at least the foregoing reasons, it is submitted that all pending claims of this application are in condition for allowance and such a Notice, with allowed claims 10-26, earnestly is solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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